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THE SEMIAUTOMATED TEST SYSTEM:
A TOOL FOR STANDARDIZED PERFORMANCE TESTING

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13. ABSTRACT

For performance tests to be truly standardized, they must be administered in a way that will minimize variation due to operator intervention and errors. Through such technological developments as low-cost digital computers and digital logic modules, automatic test administration without restriction of test content has become possible. A Semiautomated Test System (SATS), incorporating programmable digital logic modules for control, has been developed to allow an experimental psychologist, unassisted and with a minimum of special training, to set up and modify tests or experiments; thus, it is especially useful for exploratory studies. The structure of the SATS is described and an example is presented to clarify the operations involved in its use.

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INTRODUCTION

Psychologists interested in dynamic ("performance") testing have long had a need for automated performance-test devices to assure standardization of procedures. As Rosenthal (3) has pointed out, subject-experimenter interactions, even though seemingly innocuous, may greatly influence subject performance. Prior to the development of a true technology of automation, however, adequate methods to assure test standardization were very elusive. Even the sophisticated devices made possible by advanced vacuum-tube technology often lacked the long-term reliability required.

Reliable testing devices became possible with the development of semiconductor electronics, but they were typically very limited in scope, since each was constructed specifically for a single test or small group of similar tests. They were also quite expensive since it was necessary to engineer a new device for each new test. Only the relatively recent development of low-cost computers and digital logic modules has made feasible a system approach to the performance-testing problem. These devices allow extremely precise control of the testing situation and are, at the same time, quite versatile (1, 4).

Psychologists at the Naval Aerospace Medical Institute have constructed a computer-controlled performance-test system (the Automated Performance Test System) in which a time-sharing computer is used (5). This is a very flexible system that will eventually allow fully automated and standardized dynamic testing. The modular testing booths are quite suitable for the administration of a complete performance-test battery and of very complex tests employing visual, auditory, and perhaps even haptic stimuli and a variety of response modes. While the system is quite adaptable to use in continuing research programs, a considerable lead time and a great deal of outside support are required due to the intricacies of programming time-sharing computers. Thus, it is not well suited to those short-term exploratory studies that investigators find essential to the early development of a new idea. Furthermore, it is wasteful to use this expensive system for the routine administration of simple performance tests. These two considerations have led to the development of the Semiautomated Test System (SATS).

A partitioned test unit is incorporated into SATS to eliminate visual interference, and either specially designed test modules or conventional table-top devices can be used, as appropriate. SATS is adaptable to most conventional visual or auditory tasks, although extremely complex displays cannot be presented. Tests incorporating such displays are more easily administered in a larger system, such as the Automated Performance Test System (APTS).

The basic control mechanism of SATS consists of programmable digital logic modules, with various timers, counters, drum programmers, and the like, easily adaptable to the system. To increase the flexibility of the laboratory's testing facilities, provision has been made for controlling any or all of the SATS test unit stations with an APTS computer interface and for administering simple tests in any or all APTS booths under control of the SATS logic gear. Scores can be recorded on a digital paper-tape printer, or by hand from counters or other displays controlled by the digital logic circuits in use.

The SATS has been designed primarily for simplicity of use. It can be set up for a test or research project by the research psychologist alone, with a minimum of special training and outside assistance. The system is not an automated one in the sense that, once set up, it is independent of the operator; nonetheless, completely standardized performance testing can be accomplished with a minimum of variation in the task due to outside influences. The logic gear can be programmed to provide immediate scoring when desired.

TEST UNIT

The test unit (Figure 1) consists of eight booths for testing eight subjects independently. A test module may be a specially designed unit (Figure 2a) which is substituted for the desk-top in a booth, or a conventional table-top device (Figure 2b) which is placed on the desk-top. Fifty-four wires control each test module, and power is provided at two polarities (positive or negative with respect to ground) and three voltage levels (5 V dc, 12 V dc, and 24 V dc). Individual audio instructions and auditory tasks are given through stereo headsets provided for each booth. A single shielded circuit terminates in each booth for physiological measures or any other application requiring high noise immunity. The test-unit wiring runs from a small chassis box in each booth to a master connector panel at one end of the unit.

It should be emphasized that each booth is entirely independent of all other booths, so that eight different performance tests can easily be administered simultaneously in the test unit. The unit is collapsible for storage.

CONTROL UNIT

A block diagram of the entire unit is shown in Figure 3. Basically, preparation of the system for the administration of a specific test is accomplished by appropriate wiring of an audio patch panel, a master plugboard, a logic plugboard, and, when used, a physiological patch panel.

AUDIO PATCH PANEL

The audio patch panel (Figure 4) allows administration of audio instructions or auditory tasks to any of the eight SATS booths or the four APTS booths from any source (tape recorders, operator microphone, etc.). An option which allows the operator to monitor audio instructions is also available.

MASTER PLUGBOARD

This removable plugboard serves as a switchboard for all communications with any test module, whether controlled by the programmable digital logic modules, a computer interface, drum programmers, an instrumentation tape recorder, or any other device. Separation of this function from the logic plugboard is due primarily to considerations of size.

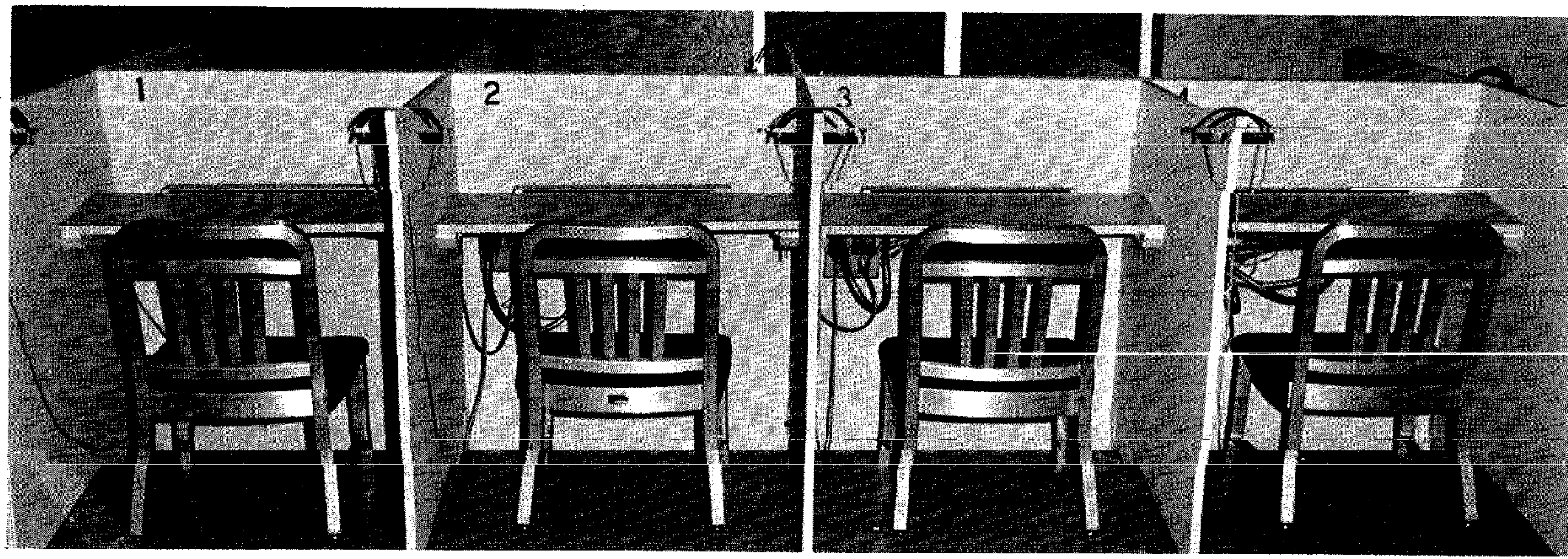

Figure 1

SATS Test Unit

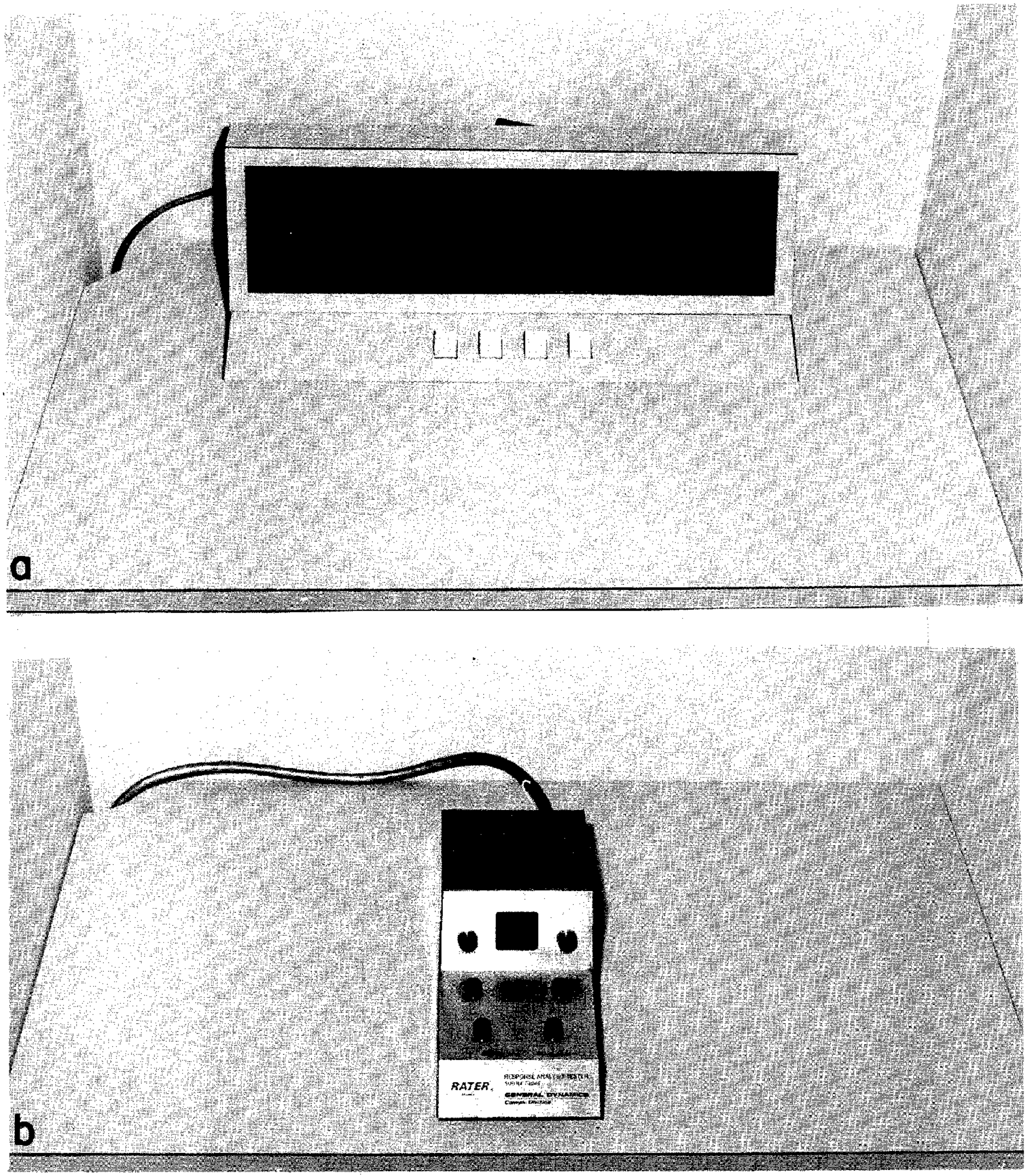

Figure 2

Test Modules

a: A specially designed test module can be substituted for the desk surface, or
b: A conventional table-top device can be used.

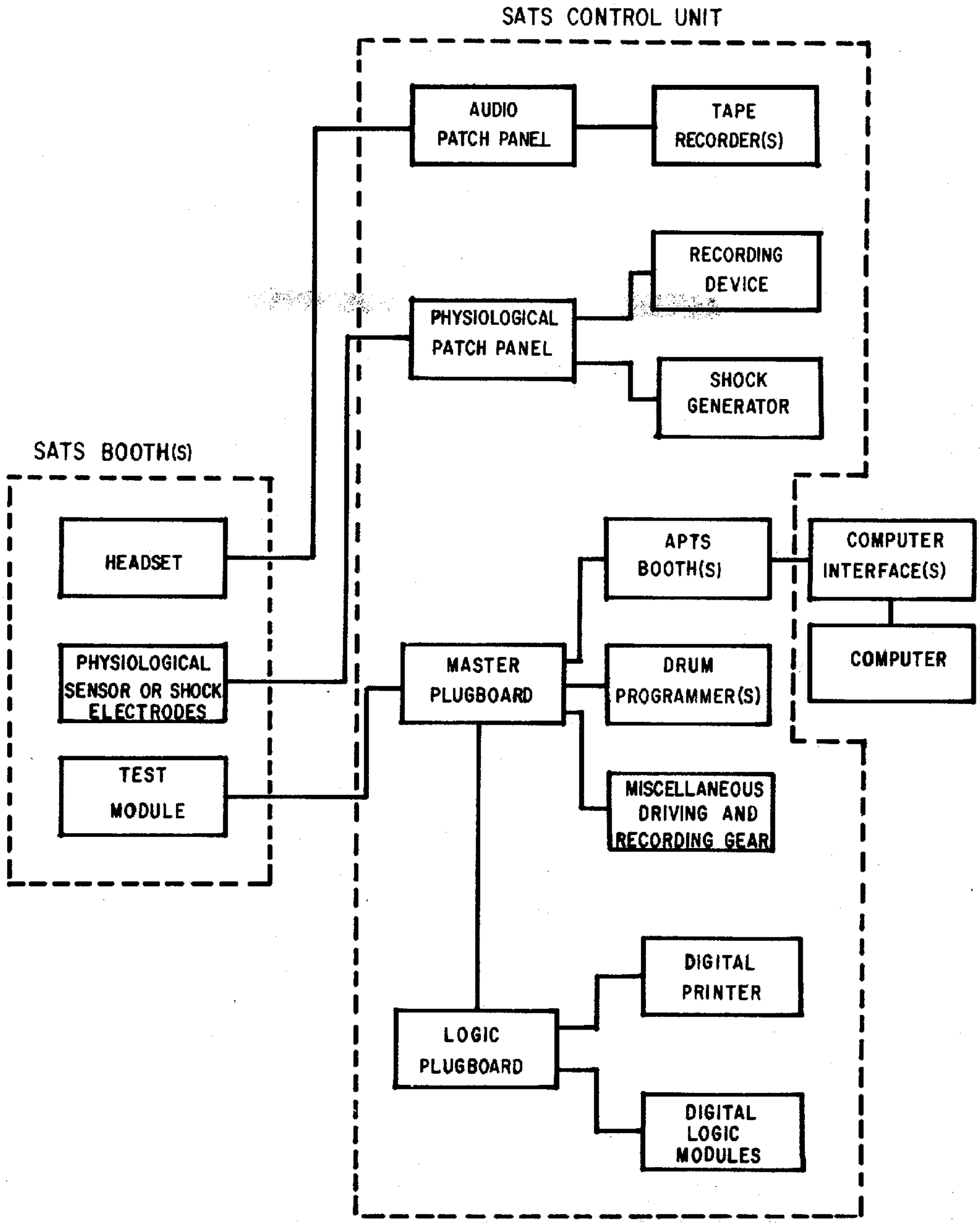

Figure 3

Block Diagram of SATS

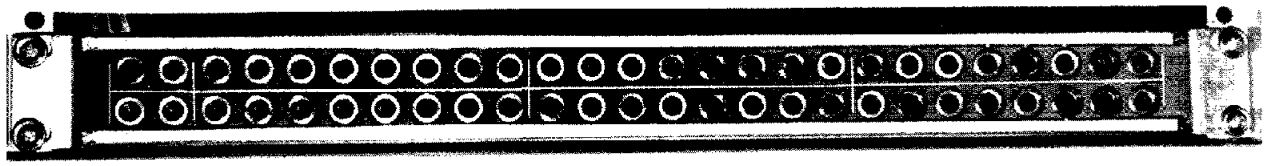

Figure 4

Audio Patch Panel

As many as five audio sources provide sound for 8 SATS booths ([redacted]) and 4 APTS booths [redacted]

The master plugboard is partitioned into 6 x 10 blocks (Figure 5). Only the first 54 positions of each block are used. Blocks A1 through A4 terminate at each of the four APTS booths, with two cables (e.g., A1a, A1b) allocated to each booth. Blocks S1 through S8 terminate at SATS booths 1 through 8, respectively. Blocks L1 through L12 terminate in correspondingly numbered areas of the Logic plugboard. The remaining positions are available for auxiliary (Miscellaneous) devices, such as drum programmers.

LOGIC PLUGBOARD

The logic plugboard (Figure 6) is the heart of the system. It allows for readily modifiable and interchangeable circuits to be constructed from BRS-Foringer Series 200 digital logic cards (Figure 7). These cards contain such logic elements as flip-flops, and-gates, or-gates, one-shots, and decade counters, as well as lamp drivers, relay drivers, indicator lamps, and input circuits. The system is based on a positive-ground, positive-logic configuration, and is designed and documented for ease of use by behavioral scientists and others not necessarily skilled in digital logic applications. Ray (2) has provided a thorough introduction to the use of these logic modules in circuit construction.

Plugboard blocks B1 through B8 (Figure 6) correspond spatially to the eight rows of BRS-Foringer logic cards shown in Figure 7. Blocks 1 through 12 terminate in the master plugboard. Blocks 13 and 14 are available for miscellaneous functions, while blocks 15 and 16 terminate at a Hewlett-Packard 5050B paper-tape printer (upper left, Figure 7), the primary output device for the system. This printer is operated directly by the logic cards, without intervening amplifiers or level converters. Print command inputs are active, requiring only a leading or trailing edge, while character control inputs are passive and require a steady voltage level for an entire print cycle (approximately 0.05 sec). Each of the 18 print columns is controlled by four inputs, with binary codes 0000, 0001, 0010, ... 1111, corresponding to print characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, +, -, V, A, Ω, *, respectively. Since the numeric characters are coded in a binary-coded decimal format, a decade counter can be used to directly control print characters in counting applications (for displaying trial number, reaction time, etc.).

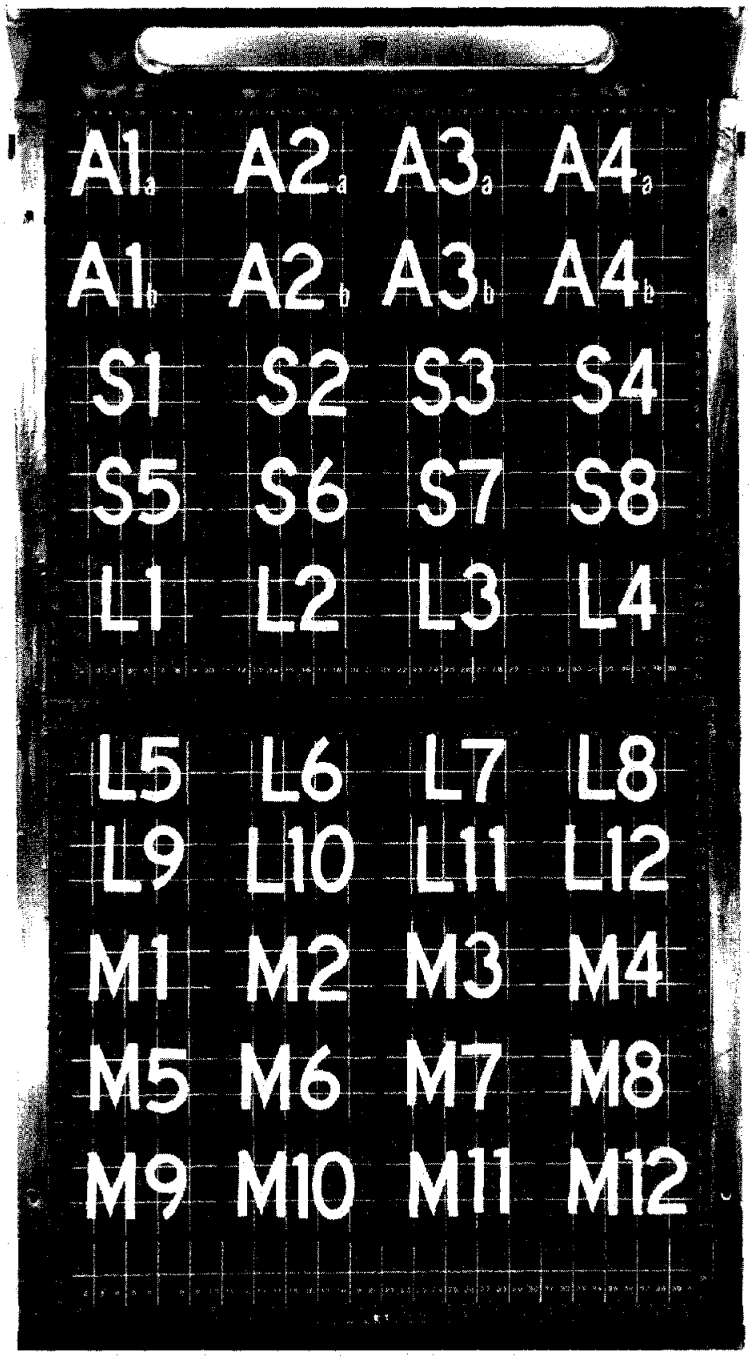

Figure 5

Master Plugboard

Blocks A1 through A4 connect with the four APTS booths, S1 through S8 with the SATS booths. Blocks L1 - L12 connect with the logic plugboard. Blocks M1 - M12 are for miscellaneous devices.

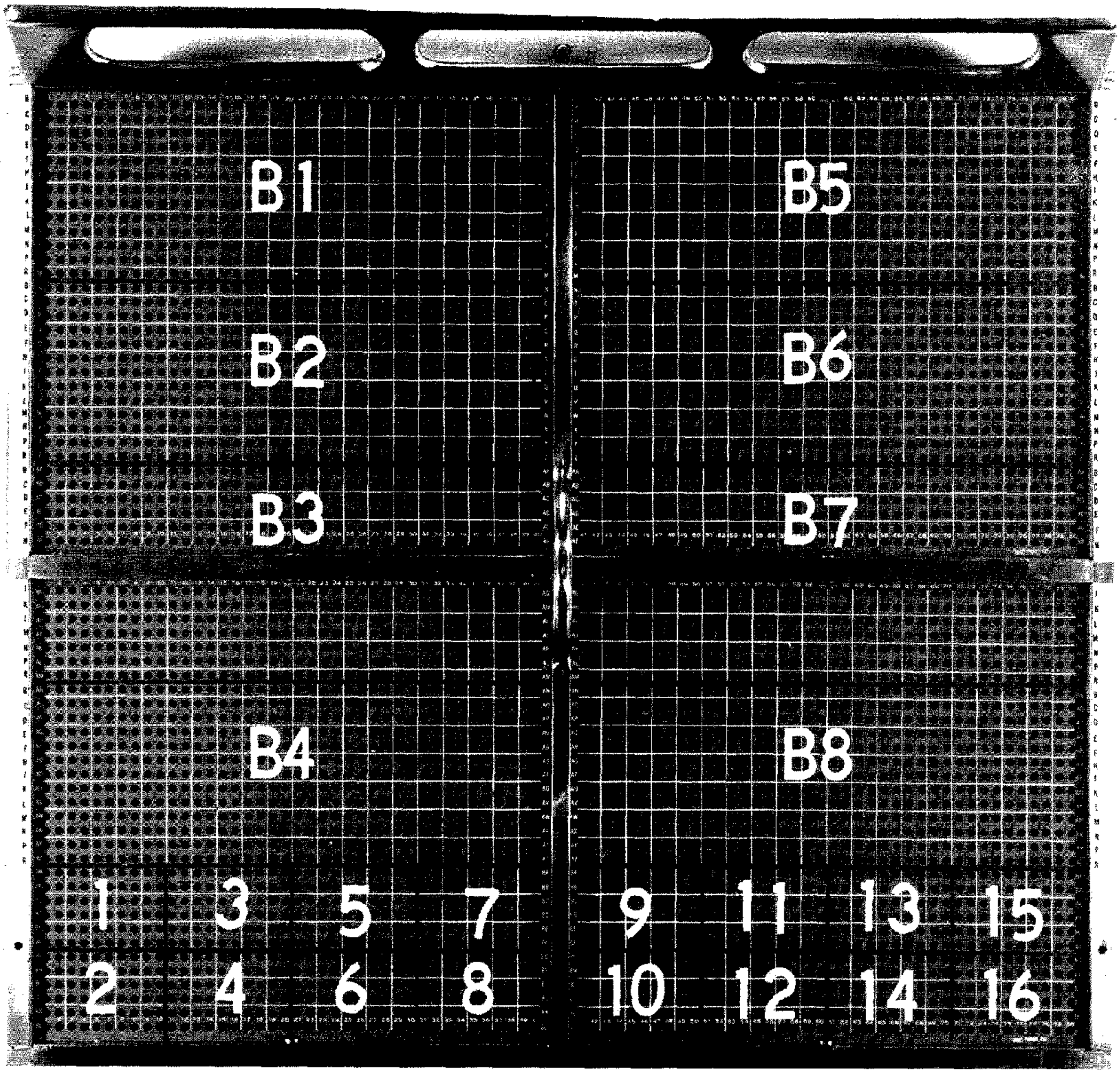

Figure 6

Logic Plugboard

Blocks B1 through B8 connect with the logic modules. Blocks 1-16 connect with the master plugboard and all system input/output devices.

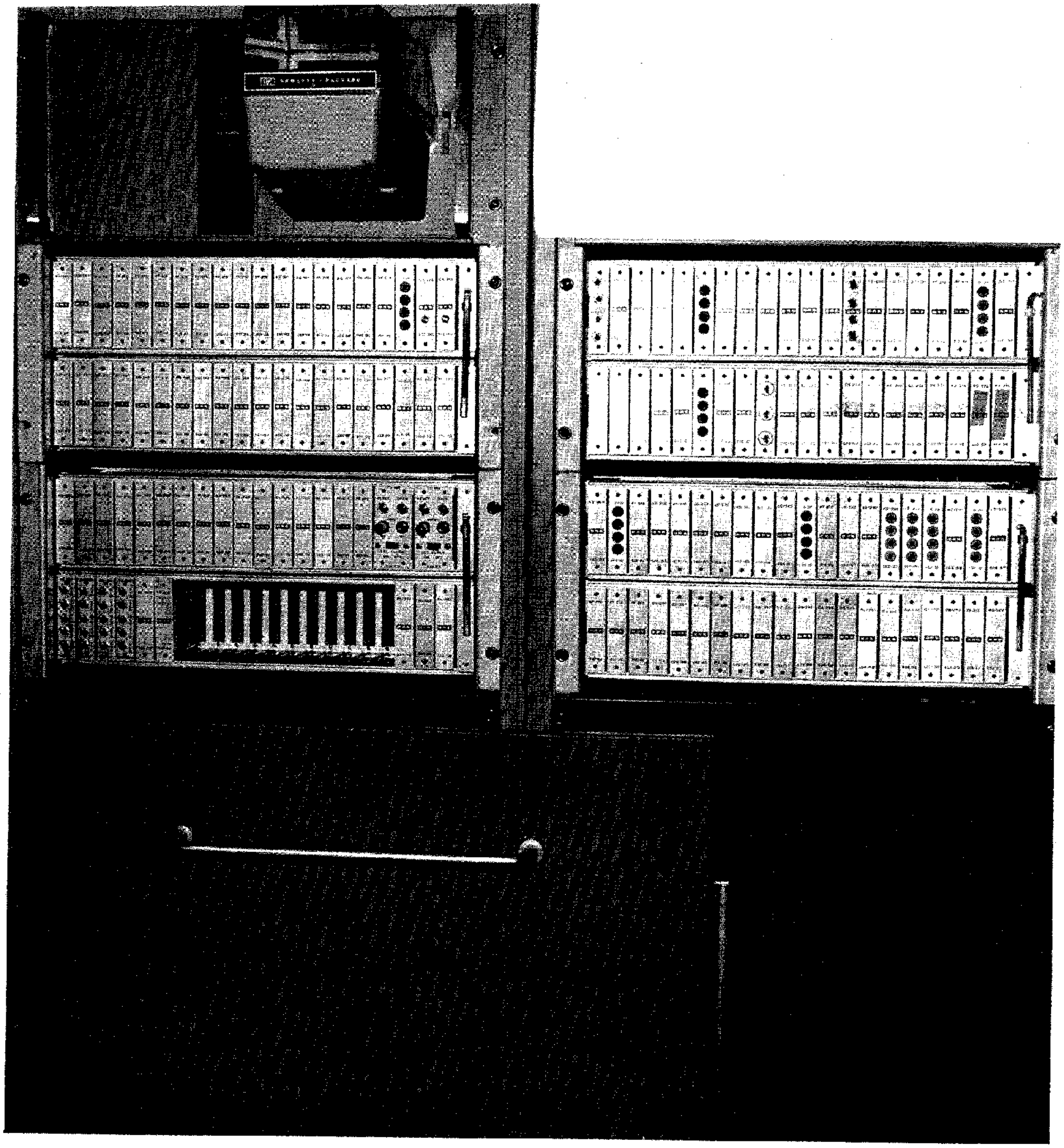

Figure 7

Logic Modules

With logic plugboard receiver (bottom) and digital printer (upper left).

PHYSIOLOGICAL PATCH PANEL

This panel provides for each booth a single electrically shielded circuit for any desired use. Anticipated uses are such physiological measures as galvanic skin response, cardiac rate, and blood pressure. The circuits can also be used to administer electric shock for conditioning or stress studies.

EXAMPLE

The procedures necessary to administer a continuous four-choice disjunctive reaction-time test will be outlined incorporating a special-purpose test module (Figure 2a) which contains, among other things, a small field that can be illuminated in any of four colors, and four response keys that can be correspondingly illuminated. The test is one in which a single color appears in the field and the subject is required to press the corresponding key. The stimulus color, the subject's response, and his reaction time are recorded and the next stimulus presented after a short interstimulus interval. On each trial the color presented is randomly chosen from the entire set of four. Repeated presentation of the same color is allowed in order to keep the example as simple as possible.

The steps required to set up this test may be performed in any order, and are:

1. Installation of the test module in the SATS test unit, including electrical connections.

2. Preparation of an audio instruction tape and connection of SATS booth to the tape recorder.

3. Wiring of the master plugboard. In this case, since the test is controlled by the digital logic modules, the master plugboard is used merely to connect the test module to the logic plugboard.

4. Wiring of the logic plugboard. An annotated flow chart such as that shown in Figure 8 may be helpful in translating the test into a digital circuit. A logic circuit appropriate for this test is shown in Figure 9. In some respects circuit efficiency has been sacrificed for the sake of clarity. Lamp drivers for the illumination of response keys have been omitted from the diagram since they remain illuminated throughout the test. Flip-flops FF1 and FF2 make up a 2-bit binary counter driven by a 1000-Hz multivibrator through and-gate A1. It is assumed that 1 msec is a sufficiently short interval relative to the subject's reaction time that the state of this binary counter at the instant of response is random. The output of this random-number generator is decoded by and-gates A2, A3, A4, and A5, and stored in flip-flops FF3, FF4, FF5, and FF6. The four decade counters in the upper right portion of the diagram constitute a four-digit millisecond timer that is also driven at 1000 Hz through and-gate A1.

For the purpose of a functional description of the circuit, it will be assumed that the test is already under way. A stimulus light is on, the millisecond timer and

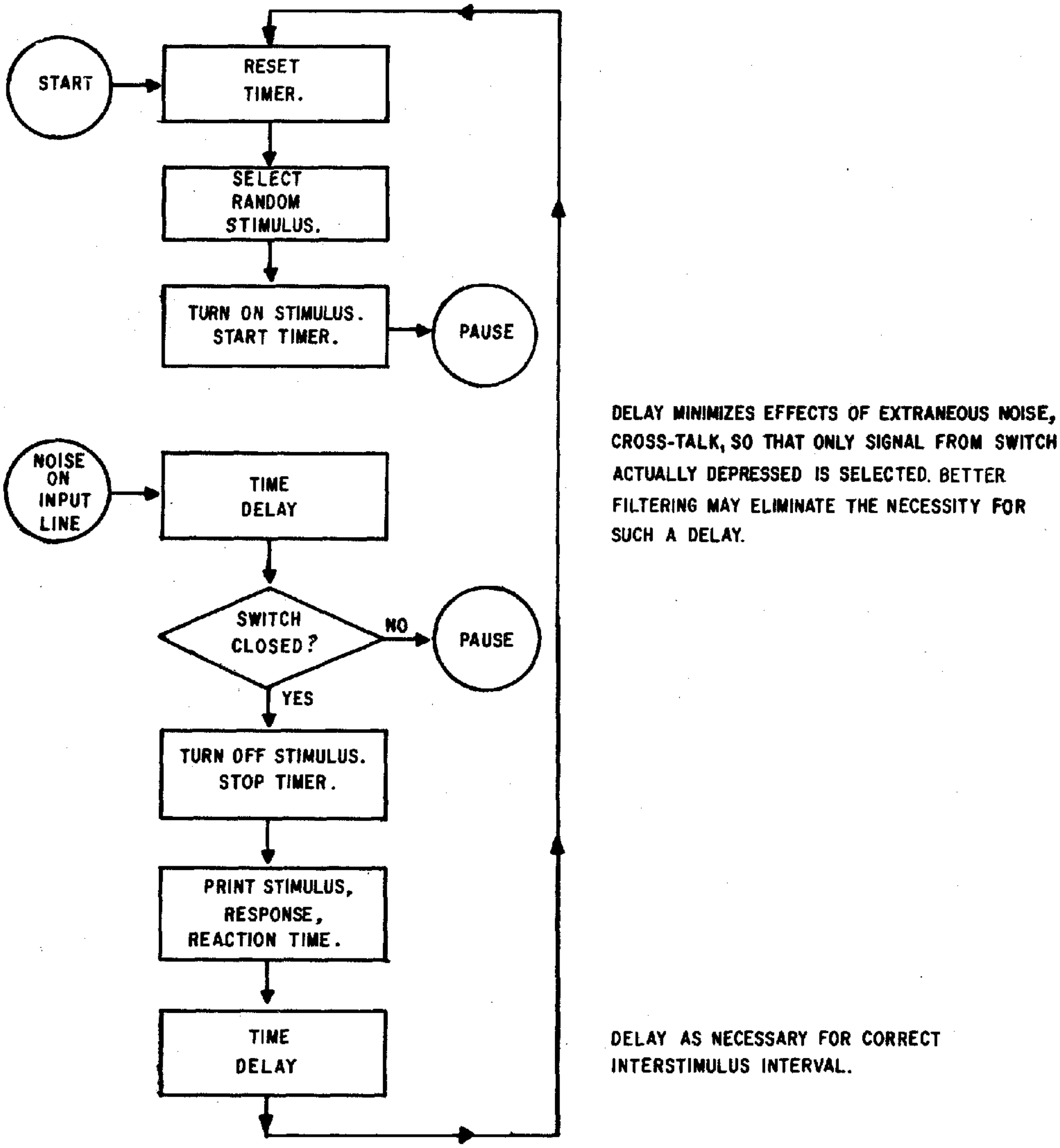

Figure 8

Flow Chart of Digital Circuit Functions for Continuous Disjunctive Reaction-Time Test

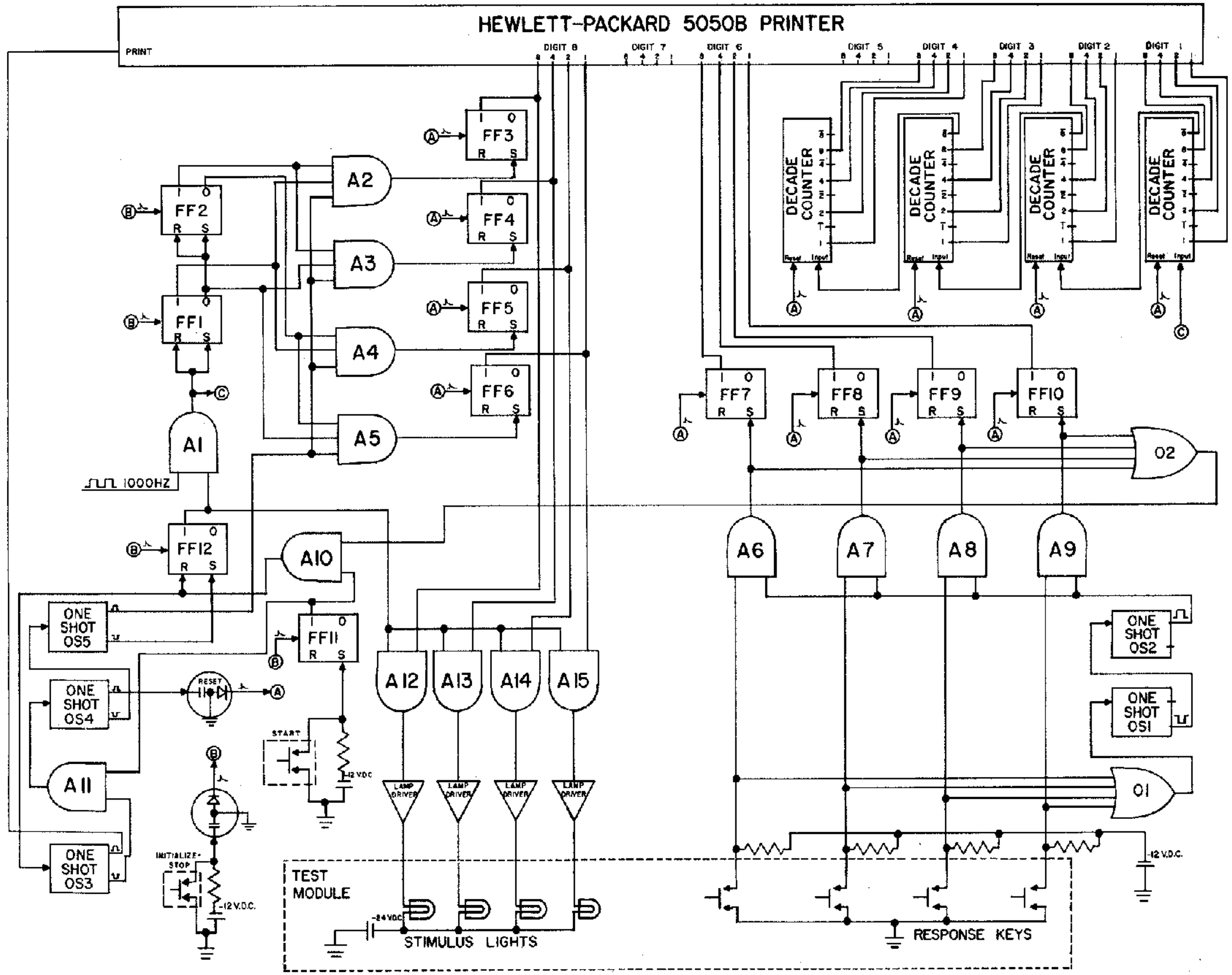

Figure 9

Digital Logic Diagram for Continuous Disjunctive Reaction-Time Test

The diagram includes a random-number generator (upper left), millisecond timer (upper right), subject response circuit (lower right), and control circuit (lower left).

random-number generator are running, and the system is awaiting a response by the subject. When the subject depresses one of the response keys, the voltage level applied at one leg of or-gate 01 and one leg of one of the and-gates A6, A7, A8, or A9 changes from from -12 V dc (logic "0") to 0 V dc (logic "1"). If this voltage level is maintained for the period determined by one-shot OS1, one of the flip-flops FF7, FF8, FF9, or FF10 is set, and the output of or-gate 02 is temporarily "on." If the circuit is in "run" mode (i.e., flip-flop FF11 is on, as assumed), and-gate A 10 is also temporarily "on," resetting flip-flop FF12 and firing one-shot OS3. With FF12 reset, both the random-number generator and the millisecond timer are stopped, and the stimulus light is off. OS3 causes the printer to record the information provided by the timer and stimulus and response flip-flops. OS3 "on" time must be at least 0.05 second (the print-cycle interval) and can be longer if a longer interstimulus interval is desired. When OS3 returns to the "off" state, OS4 is activated, resetting the timer and all stimulus and response flip-flops. OS5 then causes the new random stimulus to be stored in the stimulus flip-flops. The return of OS5 to the "off" state sets FF12, starting the timer and random-number generator and turning on the new stimulus. Readers experiencing difficulty in tracing the circuit are again referred to Ray (2).

The example is, of course, intended to be simple. With more complex circuitry the experimenter could avoid repeated stimuli, score responses as correct or incorrect, count correct responses, administer a predetermined number of trials, et cetera.

CAPABILITIES AND LIMITATIONS

The versatility of the digital logic modules is limited mainly by the number of modules available and the imagination of the experimenter. A means for entering a stimulus program such as might be desired for some tests is not presently included in the SATS. The addition of a paper-tape reader would alleviate this problem. A paper-tape punch might then be used for intermediate storage so that a test could be administered and later scored, with a consequent reduction in the amount of logic required at one time.

As presently configured, the SATS is primarily suitable for procedures involving visual stimuli, although preprogrammed auditory tests are possible. A wide variety of digital (but not, at present, analog) tests including response-contingent procedures (e.g., adaptive learning) can be administered. Specific applications now under development include reaction time, time estimation, signal detection, acquisition under a condition of information overload, vigilance, and simultaneous multiple choice testing of several subjects.

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